irradiated and crystallized since a light 17 is irradiated through the gate electrode 5G and the gate insulating film 3. Consequently, the combination of Yamazaki and Mukai does not provide the above noted feature of crystallizing at least a channel formation region of semiconductor film by laser irradiation through an insulating film. Therefore, this rejection should be reconsidered and withdrawn.

Claims 32, 53-54, 67, 69, 82, 85, 94 and claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki U.S. Patent No. 4,727,044 in view of Mukai, U.S. Patent No. 5,077,233 as applied to claims 12, 15, 17, 23, 26, 28, 34036, 46, 48, 50, 75, 77, 79, 88, and 90-91 above, and further in view of Ito et al., "Thin Film Technology of VLSI" pages 87-88. These rejections are traversed for the reasons advanced above with respect to Yamazaki and Mukai.

Specifically, Ito is merely relied upon for teaching the formation of an oxide layer using TEOS. This reference, however, fails to overcome the deficiencies of the primary references to Yamazaki and Mukai. Consequently, this rejection should be reconsidered and withdrawn.

Claims 18, 21-22, 27, 47, 76, 76 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki U.S. Patent No. 4,727,044 in view of Mukai U.S. Patent 5,077,233 as applied to claims 12, 15, 17, 23, 26, 28, 34-36, 46, 48, 50, 75, 77, 79, 88 and 90-91 above and further in view of Han et al., U.S. Patent 4,599,118. This rejection is traversed for the reasons advanced above with respect to Yamazaki and Mukai.

Specifically, Han et al. is relied upon for allegedly teaching the formation of a gate electrode with tapered sides. This reference, however, fails to overcome the deficiencies of the primary references to Yamazaki and Mukai. Consequently, this rejection should be reconsidered and withdrawn.

Claims 16, 19, 29-31, 33, 41-43, 49, 52, 58, 60-61, 68, 78, 81, 84, 87, 93, and 96 are rejected under 35 U.S.C. 103(b) as being unpatentable over Yamazaki U.S. Patent No. 4,727,044 in view of Mukai, U.S. Patent 5,077,233 as applied to claims 12, 15, 17, 23, 26, 28, 34-36, 46, 48, 50, 75, 77, 79, 88 and 90-91 above, and further in view of Chang, U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology". This rejection is traversed for the reasons advanced above with respect to Yamazaki and Mukai.

Specifically, Chang is relied upon for allegedly teaching the introduction of boron into a semiconductor layer, and Wolf et al. is relied upon for allegedly teaching that layers are deliberately added to reduce damage to a semiconductor surface. Moreover, as previously asserted, Wolf et al. fails to teach or suggest that these layer are ever removed. In view thereof, these references fail to overcome the deficiencies of the primary references to Yamazaki and Mukai. Consequently, this rejection should be reconsidered and withdrawn.

Claims 24, 55-57, 71, 83, 86 and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki U.S. Patent 4,727,044 in view of Mukai U.S. Patent 5,077,233 and further in view of Chang U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology" as applied to claims 16, 19, 29-31, 33, 41-43, 49, 52, 58, 60-61, 68, 78, 81, 84, 87, 93 and 96 above, and further in view of Ito et al., "Thin Film Technology of VLSI", pages 87-88. For the reasons advanced above with respect to the primary references to Yamazaki and Mukai and the secondary references to Chang, Wolf et al., and Ito et al., this rejection should likewise be reconsidered and withdrawn.

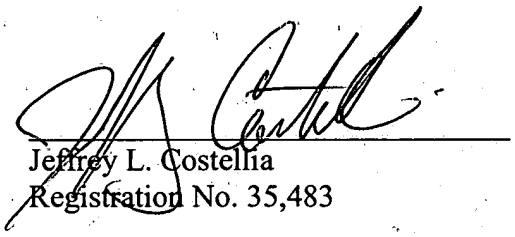
Claims 13, 37-40, 51, 80 and 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki U.S. Patent 4,727,044 in view of Mukai U.S. Patent 5,077,233 and further in view of Chang U.S. Patent 5,064,775 and Wolf et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology" as applied to claims 16, 19, 29-31, 33, 41-43, 49, 52, 58, 60-61, 68, 78, 81, 84, 87, 93 and 96 above, and further in view of Han et al., U.S. Patent 4,599,118. For the reasons advanced above with respect to the primary references to Yamazaki and Mukai and the secondary references to Chang, Wolf et al., and Han et al., this rejection should likewise be reconsidered and withdrawn.

Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki U.S. Patent 4,727,044 in view of Mukai U.S. Patent 5,077,233 and further in view of Chang U.S. Patent 5,064,775 and Wolfe et al., "Silicon Processing for the VLSI Era Volume 1: Process Technology" and Han et al., U.S. Patent 4,599,118 as applied to claims 13, 37-40, 51, 80 and 92 above, and further in view of Ito et al., "Thin Film Technology of VLSI", pages 87-88. For the reasons advanced above with respect to the primary references to Yamazaki and Mukai and the secondary references to Chang, Wolfe et al., Han et al. and Ito et al., this rejection should

likewise be reconsidered and withdrawn.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 12, 13, 15-19, 21-24, 26-43, 46-58, 60, 61, 65-71 and 75-96 be allowed, and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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